REMARKS/ARGUMENTS

The present application contains claims 1-6, 8, 9, 11 through 18, 21, 24, 25, and 28-31. Claims 4, 11, 14-17, 21 and 24 have been withdrawn from prosecution as being directed to non-elected subject matter. Claims 7, 10, 20 and 22 were previously canceled and claims 19, 23, 26 and 27 have been canceled by way of this amendment without prejudice to Applicant in order to expedite the prosecution of the present application. Claims 1, 13, 30 and 31 have been amended by this amendment.

The specification has been amended to conform the text to the figures.

The rejection of claims 1, 2, 12, 13, 18, 19, 23, 26, 27, 30 and 31 as failing to comply with 35 U.S.C. Section 112, 2nd Paragraph is respectfully traversed as regards claims 1, 2, 12, 13, 18, 30 and 31, claims 19, 23, 26 and 27 having been canceled without prejudice to Applicant in order to expedite the prosecution of the present application.

Regarding claim 1, this claim has been amended to recite the step of introducing a current to said parasitic capacitance to prevent the parasitic capacitance from drawing current from said input signal responsive to detection of a positive edge of said input signal. It is submitted that claim 1 is now definite. Note, for example, the last three lines appearing on page 1 of the specification which clearly support the amendment made to claim 1.

Regarding the issue of claims 12 and 13, claim 13 has been amended to replace the phrase "positive edge" to read "negative edge" in order to cure the confusion regarding claims 12 and 13.

Regarding claims 30 and 31, the phrase "the first mentioned circuit" has been amended to recite "said circuit operating at high frequency" which finds antecedent basis at line 2 of claim 5 which recites "a circuit operating at high frequency".

For the above reasons it is submitted that claims 1, 2, 12, 13, 18, 30 and 31 now comply with 35 U.S.C. Section 112 and it is submitted that this rejection should be withdrawn.

It is noted that claims 2 and 18 have been considered to be indefinite because of the technical deficiencies of claim 1. Due to the amendment of claim 1, it is submitted that claims 12 and 18 are now definite.

Claims 1-3, 5, 6, 8, 9, 12, 13, 23, 25, 26 and 28-31 have been rejected under 35 U.S.C. Section 102 (b) as anticipated by Bruccoleri et al. (Patent '488). This rejection is respectfully traversed as regards claims 1-3, 5, 6, 8, 9, 12, 13, 23, 25 and 28-31, claims 23 and 26 having been canceled without prejudice to Applicant in order to expedite the prosecution of present application.

It is submitted that Patent '488 does not teach a method for reducing distortion of a signal to an input of an input/output device having parasitic capacitance between said input and ground.

Patent '488 is specifically limited to teaching a bi-stable latch with, as shown in Fig. 3, has two inputs and not merely one input note VIN+ and VIN-.

The operation of the bi-stable latch is such that the input signals, which are taken from a differential amplifier DIF shown in Fig. 1 of Patent '488, are respectively applied to the Z+ and Z- inputs by closing electronic switches S1 and S2. It is **important** to note that electronic switches S3 and S4 are **open** at the time that switches S1 and S2 are closed. During this "sampling" phase of operation it is clear that the inverters INV1 and INV2 **cannot operate**. The switches S1 and S2 are closed for a time sufficient to "charge the input capacitances C_{IN} of the two inverters." See column 3, lines 37 and 38 of Patent '488. In entering the next or evaluation phase switches S1 and S2 are open and switches S3 and S4 are closed to supply inverters INV1 and INV2 enabling the positive feedback between them to be active. At this time the inverters **do not** see a positive going signal but see a steady level since, during the sampling phase, the input capacitances CIN at the inputs Z+, Z- have had an opportunity to become **fully charged** to the input voltages VIN+ and VIN-.

Thus, the inverters IV1 and IV2 do not see positive or negative edges of an input signal but, to the contrary, see a constant voltage signal. As a result it is submitted that there is neither teaching nor remote suggestion in Patent '488 of a means for preventing distortion of a high frequency signal applied to an input of a

circuit operating at such high frequency. The embodiment of Figure 3 of Patent '488 teaches the use of electronic switches S3 and S4 for the purpose of discharging capacitances C_A and C_B to further prevent initiation of positive feedback during the sampling phase. This arrangement reinforces and confirms the argument that there is no positive feedback during the sampling phase which is further assured by use of the electronic switches S3 and S4 and the timing of the use of these electronic switches **in addition to** decoupling power from inverters INV1 and INV2 during the sampling phase.

For the above reasons it is submitted that claims 1, 2, 12, 13, 18, 27, 30 and 31 patentably distinguish over Patent '488 since there is neither teaching nor remote suggestion of "introducing a current to said parasitic capacitance to prevent said parasitic capacitance from drawing current from said input signal responsive to detection of a positive edge of said input signal" such as is recited in claim 1 and "preventing discharge of said parasitic capacitance into the input of said circuit responsive to detection of a negative edge of said input signal," as recited in claim 3. Claims 12 and 13 recites similar limitations and claims 2, 18, 30 and 31 all depend from one of the aforesaid independent claims and hence are deemed to patentably distinguish over the '488 Patent.

Claims 1, 2, 5, 6, 12, 18, 25 and 26 have been rejected under 35 U.S.C. Section 102(e) as anticipated by Diniz et al. (Patent '868). This rejection is

respectfully traversed as regards claims 1, 2, 5, 6, 12, 18 and 25, claim 26 having been canceled without prejudice to Applicant in order to expedite the prosecution of the present application.

Diniz is limited to teaching a device, typically referred to as a current mirror, whose function is to provide a steady constant output current which is insensitive to temperature, supply voltages and the like as per column 3, lines 1-5.

To the contrary, the present invention is directed to correcting/preventing distortion of a **high frequency signal** which distortion is caused at such high frequencies by the parasitic capacitance of the input to the circuit receiving the high frequency signal.

It is thus not seen how a teaching of a current mirror device which is in the field of technology quite remote from the high frequency application of the present invention can be looked to for teaching the technology of the present invention and it is submitted that one having ordinary skill in the art would not seek solutions to the invention of the present application in such remote art as current mirrors.

Making reference to Figure 3 in Patent '868, it should be noted that the sensitivity of the circuit shown therein is to temperature and **not** to frequency. The two components which are temperature sensitive include transistor 44 and resistor 42. See column 2, lines 39-42 of Patent '868. The objective of the invention in Patent '868 is to compensate for unwanted changes in the output current 91 due to

the effect of temperature on the threshold voltage V_t of transistor 44 and due to the effect on the resistance value of resistor 42. There is neither teaching nor remote suggestion of use of any of the circuit design shown in Patent '868 for preventing distortion of a high frequency input signal to an input of a high frequency circuit. It should be noted that, although Patent '868 recognizes the fact that there is a gate oxide capacitance per unit area of transistor area 44 (see column 2, lines 1-13), the value of the square root term in equation (1) at the top of column 2 is **neglected** for purposes of analysis of the '868 invention. This is the only instance in the text of the '868 Patent where a capacitance is mentioned and it is clear that its value is neglected by simply choosing a ratio of channel width to channel length of transistor 44. See column 2, lines 13-20. The startup circuit 72 shown in Fig. 3 is clearly **not** a high frequency input but merely a circuit for injecting a starting **current** into the structure of the circuitry to ensure that the current source is driven to its stable operating point. See column 2, lines 30-36. The operation of the circuit of Figure 3 is such that resistor 42 determines the current 66 flowing through transistors 49 and 48 and resistor 42. The voltage across transistor 42 is equal to the current flowing through resistor 42 times its resistance. This is equal to the threshold voltage V_t applied to the gate of transistor 44 which determines the current 64. Reference current 64 and current 66 are substantially equal in the current mirror 60. See column 1, lines 59-66. Any changes in the voltage Vt is applied to

transistor 99 which controls the current 120 in current mirror 100. In current mirror 100, current 84 is equal to current 120. Any drop in current 82 in current mirror 62 is compensated for by an increase in current 84 causing the sum of currents 82 and 84 (namely current 85) to be constant. Even assuming for the sake of argument that there is a parasitic capacitance between the gate and source of transistor 48, there is no teaching or even remote suggestion of compensating for the effect of the parasitic capacitance upon the input signal responsive to detection of a positive edge of the input signal, in the case of claim 1, for example.

The Examiner, in reading the claims on Figure 3 of Patent '868 states that:

a direction of change of the input voltage is detected at the input or gate of transistor 48;

introducing a current 64 when a positive edge of the input signal is applied to the gate of transistor 48 to charge the parasitic capacitance, not shown and inherently exists between the gate and the source of transistor 48 to compensate the current of the input signal charging the parasitic capacitance.

In order for the circuit of Figure 3 in Patent '868 to operate in the manner proposed by the Examiner, the detection of the signal applied to the input passes through transistor 48 to change the current 66. Thus the distortion has already been introduced into the "input" (i.e., the gate electrode of transistor 48). None of the transistors 46, 44 and 49 are capable of detecting a positive going edge of a

signal. Transistor 49 is **not** directly coupled to the gate electrode of transistor 48. The gates of transistors 44 and 46 are not coupled to the "input" gate electrode of transistor 48 and hence these transistors are not capable of detecting a positive edge in the signal.

Summarizing, Patent '868 neither teaches nor remotely suggests any circuitry for compensating for distortion in a signal applied to an input of a circuit by introducing a current into the parasitic capacitance upon detection of a positive going edge of said signal.

This also applies to preventing discharge of a parasitic capacitance into the input of the circuit responsive to detection of a negative edge of the input signal, as is recited in claim 3.

Also as was set forth hereinabove, it is submitted that the technology of Patent '868 is remote from the technology of the present invention and it is submitted that it would not have been obvious to one having ordinary skill in the art at the time of the invention of the present application to look to the '868 Patent as a basis for arriving at the teachings of the present invention.

In view of the foregoing, it is submitted that claims 1, 2, 5, 6, 12, 18 and 25 patentably distinguish over Patent '868.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-3, 5, 6, 8, 9, 12, 13, 18, 25 and 28-31 patentably distinguish over the cited art of record and reconsideration and allowance of these claims are earnestly solicited.

If the Examiner believes that any additional minor formal matters need to be addressed in order to place this application in condition for allowance, or that a telephone interview will help to materially advance the prosecution of this application, the Examiner is invited to contact the undersigned by telephone at the Examiner's convenience.

In view of the foregoing amendment and remarks, Applicants respectfully submit that the present application, including claims 1-3, 5, 6, 8, 9, 12, 13, 18, 25 and 28-31, is in condition for allowance and a notice to that effect is respectfully requested.

Favorable action is awaited.

Respectfully submitted,

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